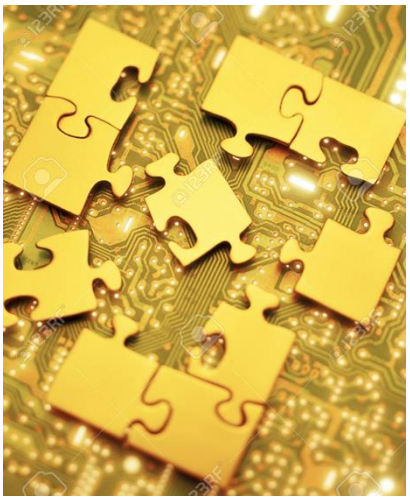
ECE 2411: Logic Circuit II

Every Semester

Instructor:	Dr. Byeong Kil Lee
Class hours:	Mon/Wed 10:50am-12:05pm
Classroom:	ENGR 136
Office:	AEC 304
Office hours:	Mon/Wed: 3pm-4pm or by appointment
E-mail:	blee@uccs.edu
URL:	http://faculty.uccs.edu/blee

Course Description: Learn design and implement synchronous sequential logic circuits. Mealy and Moore machine, states assignment, state reduction and encoding. Verilog HDL as modeling and verifying tool for both combinational and sequential logic circuits in a series of laboratories. Prer., ECE 1411; coreq., ECE 1021 or CS 2060. College of Engineering students only.

Topics to be Covered:



Prerequisites By topic:

- Combinational networks design
- Boolean minimization
- K-map and logic optimization methods

Textbook: Digital Systems Design Using Verilog, 1st Edition, 2015
(Authors: Charles Roth, Lizy K. John, **Byeong Kil Lee**), Cengage
[ISBN: 978-1285051079]

Grading:

- Homework (20%)
- Lab assignments* (20%)
- Midterm Exam (20%)
- Final Exam (30%)
- Class Participation, Pop quizzes, etc. (10%)

*Homework and Lab Assignment (4 & 4): Lab assignments include system design, Verilog coding, compile & debug, simulation, testing and analysis, etc.